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Atty Dckt Number: 2102397-911600

PATENT

#17 Appeal Brief
M. Brunsman
5/13/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Geeng-Chuan Chern

Application No. 09/916,618

Filed: July 26, 2001

For: SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH VERTICAL CONTROL GATE SIDEWALLS AND INSULATION SPACERS
(as amended)

Group Art Unit: 2814

Examiner: Howard Weiss

APPEAL BRIEF

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GRAY CARY WARE & FREIDENRICH Date: 04/28/03

By: Rosa A. Caviedes

Rosa A. Caviedes

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a brief for an appeal from a Final Office Action dated December 11, 2002, an Advisory Action dated February 25, 2003, and from a Notice of Appeal mailed on March 10, 2003. Three copies of this appeal brief are enclosed.

Real Party in Interest

The real party of interest is Silicon Storage Technology, Inc. of Sunnyvale, California, pursuant to the assignment executed on September 4, 2001, and recorded on October 15, 2001 at reel/frame 012271/0908.

05/06/2003 DTESSEM1 00000133 09916618
01 FC:1402 320.00 OP

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1-32 were originally presented on the filing of the present application. In response to the restriction requirement mailed April 23, 2002, the Applicant cancelled method claims 1-22, in favor of apparatus claims 23-32. Claims 23 and 28 have been amended. This is an appeal of the finally rejected claims 23-32. No other claims are pending or have been cancelled.

Status of Amendments

An amendment subsequent to the final rejection was mailed on January 29, 2003, which was entered by the Examiner as set forth in the advisory action mailed February 25, 2003.

Summary of the Invention

The present invention is an electrically programmable and erasable memory device, which is shown in Fig. 3M from the application, as reproduced below (in slightly modified form, with additional element numbers added for clarity):

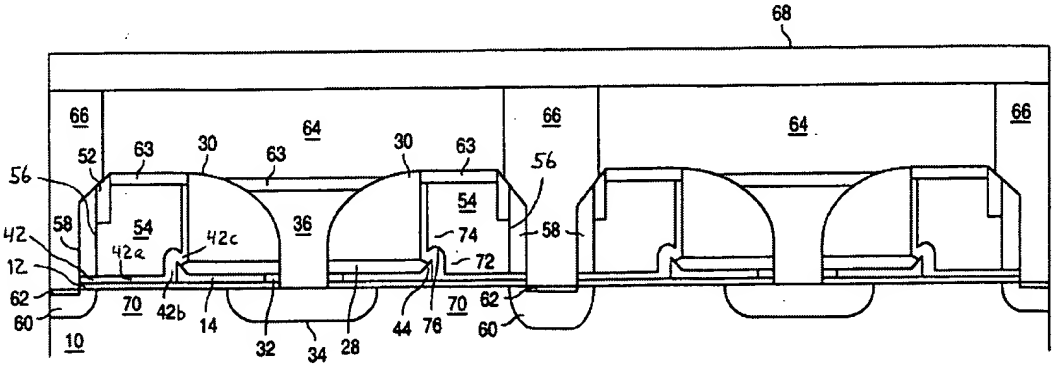

FIG. 3M

The memory device includes a plurality of programmable memory cells. As shown in Fig. 3M, each memory cell includes a source (first) region 34 and a drain (second) region 60 formed in a semiconductor substrate 10, with a channel region 70 formed therebetween. A first insulation layer 12 is formed over the substrate 10. An electrically conductive floating gate 14 is disposed over the first insulation layer 12, and extends over a portion of the channel region 70 and over a portion of the source region 34. (Page 12, lines 17-29.)

A key feature of the present invention is a second insulation layer 42 that is formed with a first portion 42a disposed over the first insulation layer 12 and the substrate 10, a second portion 42b disposed adjacent to the floating gate 14, and a third portion 42c disposed over the floating gate 14. The second insulation layer 42 has a thickness that permits Fowler-Nordheim tunneling of charges therethrough (which is used to remove electrons from the floating gate during an erase operation). (Fig. 3F; page 9, line 28 to page 10, line 5.)

An electrically conductive control gate 54 has a first portion 72 (disposed over the second insulation layer first portion 42a and adjacent to the second insulation layer second portion 42b), and a second portion 74 (extending over the second insulation layer third portion 42c). The control gate includes a substantially vertical sidewall portion 56. An insulation spacer 58 is formed adjacent to the substantially vertical sidewall portion 56 of the control gate 54. The drain region 60 has an edge that is aligned with the substantially vertical sidewall portion 56. (Page 12, lines 21-26.)

Issues

The sole issue on appeal is whether claims 23-32 are unpatentable under 35 U.S.C. 103(a) over U.S. Patent No. 5,811,853 (Wang), U.S. Patent No. 5,493,138 (Koh), U.S. Patent 6,091,104 (Chen '104), Applicant's Admitted Prior Art, Fig. 1C (AAPA), U.S. Patent No. 5,751,048 (Lee), and U.S. Patent 6,140,182 (Chen '182).

Grouping of the Claims

The claims stand or fall together.

Attachments

Attached herewith please find an appendix containing the claims involved in the appeal.

Argument

Independent claim 23 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,811,853 (Wang), U.S. Patent No. 5,493,138 (Koh) and U.S. Patent 6,091,104 (Chen '104). Independent claim 28 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 6,140,182 (Chen '182).

The applicant respectfully traverses the rejections of these two independent claims because 1) the combination of cited references fails to teach all elements of the claimed invention, and 2) there is no motivation to combine the cited references as suggested by the Examiner. The remaining claims 24-27 and 29-32 are deemed allowable for their dependence upon independent claims 23 and 28.

A. The Prior Art

The following prior art references are relied upon by the Examiner:

1. Wang (U.S. 5,811,853)

The Wang reference discloses an EPROM memory cell, as shown below in Fig. 8 of Wang (with element numbers added):

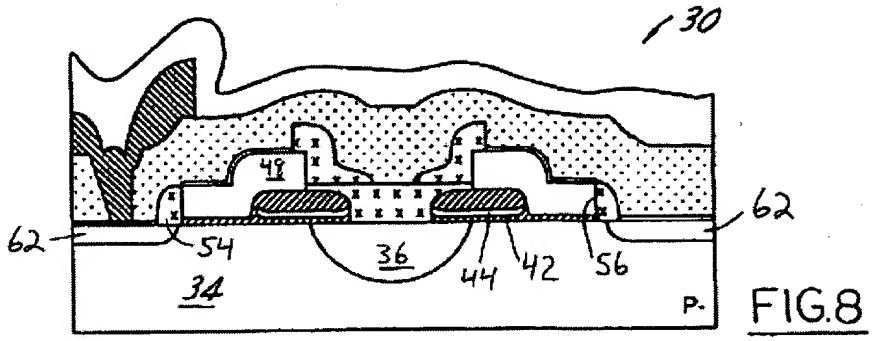

FIG.8

The Wang memory cell includes a semiconductor substrate 34, a tunneling oxide layer 42 formed on the substrate top surface, source and drain regions 36/62 of the substrate 34 with a channel region therebetween, a floating gate 44 formed on the oxide layer 42, a control gate 48 formed over the oxide layer 42 and the floating gate 44, and a spacer 54 formed on the vertical edge 56 of the control gate 48 (see Col. 4, lines 13-56).

2. Koh (U.S. 5,493,138)

The Koh reference discloses a memory device, as shown below in Fig. 8 of Koh:

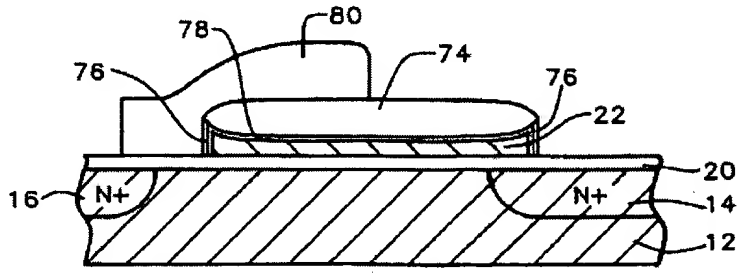

FIG. 8

The Koh memory device includes a semiconductor substrate 12, a first insulating layer 20 formed on the substrate top surface, source and drain regions 16/14 of the substrate 12 with a channel region therebetween, a floating gate 22 formed on the oxide layer 20, and a control gate 80 formed over the oxide layer 20 and the floating gate 22. Separate insulation layers 76 and 78

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($)320.00

Complete if Known	
Application Number	09/916,618
Filing Date	July 26, 2001
First Named Inventor	Geeng-Chuan Chern
Examiner Name	Howard Weiss
Art Unit	2814
Attorney Docket No.	2102397-911600

METHOD OF PAYMENT (*check all that apply*)

☒ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

Deposit Account Number: 07-1896

Deposit Account Name: Gray Cary Ware & Freidenrich LLP

The Commissioner is authorized to: (*check all that apply*)

☐ Charge (fees) indicated below. ☒ Credit any overpayments

☒ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		-3** =		X		=	
Multiple Dependent				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,300	2453	650	Petition to revive – unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 320.00

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SUBMITTED BY					Complete (*if applicable*)
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Signature				Date	April 28, 2003

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Gray Cary\EM\7140321.1

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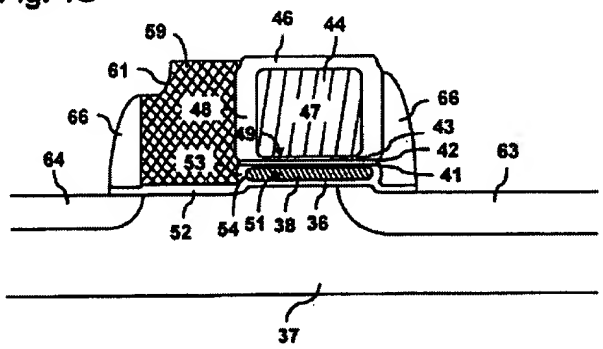
are used to insulate the floating gate 22 from the control gate 80. Insulation layers 76/78 are shown as distinct layers of material (see Fig. 8), are formed in separate processing steps (see Col. 5, lines 20-28), and are formed of different materials for superior tunneling insulation (see Col. 5, lines 35-37).

3. Chen '104 (U.S. 6,091,104)

The Chen '104 reference discloses a memory cell, as shown below in Fig. 4G of Chen '104:

Fig. 4G



The Chen '104 memory is relied upon by the Examiner for showing the alignment between a drain region 64, a select gate 59, and a spacer 66.

4. AAPA (Fig. 1C)

Applicant's Admitted Prior Art (AAPA) is relied upon by the Examiner for showing a notch formed in a control gate for a floating gate's sharp edge.

5. Lee (U.S. 5,751,048)

The Lee reference is relied upon by the Examiner for allegedly showing the alignment of conductive contacts to spacers.

6. Chen '182 (U.S. 6,140,182)

The Chen '182 reference is relied upon by the Examiner for showing isolation regions.

B. Rejection of Claims 23-24 Under § 103(a)

Claims 23-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,811,853 (Wang), U.S. Patent No. 5,493,138 (Koh) and U.S. Patent 6,091,104 (Chen '104). The applicant respectfully traverses this rejection because the combination of references fails to teach the claimed invention, and there is no motivation to combine the references as suggested by the Examiner.

1. The Wang, Koh and Chen '104 combination fails to teach or suggest the claimed insulation scheme as recited in claim 23.

Claim 23 recites that the memory device includes, among other things, a first insulation layer disposed over the substrate, a floating gate over the first insulation layer, and *a second insulation layer having three portions: "a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough".*

The Examiner rejects claim 23 over the combination of Wang, Koh and Chen '104. The Examiner admits on page 3 of the Final Office Action that Wang fails to teach a memory cell having the claimed second insulation layer, but the Examiner goes on to state:

> "Koh teaches (e.g. Figure 8) to form a tunnel insulating layer with third and second portions 78 over and adjacent, respectively, to a floating gate 22 and a first portion 76 disposed over a first insulation 20 and a substrate 12 to improve the integrity of the insulating layer between the floating gate and the control gate (Column 3 Lines 61 to 67). It would have been obvious to a person of ordinary skill in the art at the time of invention to form a tunnel insulating layer with third and second portions over and adjacent, respectively, to a floating gate and a first portion disposed over a first insulation and a substrate as taught by Koh in the

device of Wang to improve the integrity of the insulating layer between the floating gate and the control gate."

The Applicant respectfully traverses this conclusion. Claim 23 recites one insulation layer with multiple portions disposed at certain locations within the memory cell. In contrast, the insulation layers 76 and 78 of Koh are two distinct insulation layers (made of different materials and formed by different processes - Col. 5, lines 20-37). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); MPEP 2143.03. It is respectfully submitted that the two separate insulation layers 76/78 of Koh do not teach or suggest the claimed second insulation layer (having the first, second and third portions) as recited by claim 23.

In fact, Koh specifically teaches away from the Examiner's interpretation. The improvement taught by Koh is the use of a dual tunnel insulator consisting of a silicon oxide layer (76) and an inner silicon oxynitride layer (78) (see Col. 4, lines 21-23; Col. 5, lines 20-24 and 30-32), which is taught to be a much better tunneling insulator structure than just silicon oxide (see Col. 5, lines 35-37). A reference should be considered as a whole, and portions arguing against or teaching away from the claimed invention must be considered. Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 796 F.2d 443, 230 U.S.P.Q. 416 (Fed. Cir. 1986). When considering that Koh specifically teaches the importance of using two separate insulating layers of different composition, it is respectfully submitted that layers 76 and 78 of Koh cannot be deemed to meet, teach or suggest the use of an insulating layer with the first, second and third portions as recited in claim 23.

Claim 23 further recites a control gate "having a first portion disposed over the second insulation layer first portion and adjacent to the second insulation layer second portion". Even if the combination of layers 76 and 78 are implemented in the Wang device as suggested by the Examiner, there would be no portion of the control gate 48 of Wang that would be both over and adjacent to layers 76/78 (as recited in claim 23).

Thus, it is respectfully submitted that the combination of Wang and Koh do not result in, and do not teach or suggest, the claimed insulation scheme as recited in claim 23.

2. It is improper to combine Chen '104 with Wang as suggested by the Examiner.

Claim 23 also recites that "the second region has an edge that is aligned with the substantially vertical sidewall portion" of the control gate. In rejecting claim 23 in the Office Action dated June 25, 2002, the Examiner found it would have been obvious to modify the Wang device with the teaching of Chen '104 (i.e. align the edge of an impurity region with the edge of the vertical sidewall of a gate and a spacer) "to improve the performance of the device", citing Col. 3, lines 38-40 of Chen.

The Applicant responded by amendment mailed September 25, 2002, arguing that combining Wang and Chen '104 was improper because the references themselves failed provide some teaching whereby the applicant's combination would have been obvious, and the Examiner's rejection appeared to impermissibly engage in a hindsight reconstruction of the claimed invention using the applicant's structure as a template and selecting elements from references to fill the gaps. Interconnect Planning, 774 F.2d at 1143, 227 USPQ at 551. The text cited by the Examiner (Col. 3, lines 38-40) of Chen '104 is merely a general object of the disclosed invention as a whole, with no explicit or implicit reference to the alignment between the gate vertical sidewall and the impurity region, or how that feature would add benefit to other structures.

The Examiner responded to the Applicant on this issue on page 6 of the Final Office Action with the conclusion that "In this case, Chen '104 state that to align the edge of an impurity region 64 with the edge of the vertical sidewall of a gate 59 and a spacer 66 improves the performance of the device. Support for this is given in further detail in Column 5 Line 64 to Column 6 Line 19 and Column 10 Lines 43 to 67 (e.g. faster performance and small sheet size)."

This conclusion is respectfully traversed. The Applicant cannot find any such statement (relating to the alignment of the impurity region 64) in Chen '104. Moreover, the text cited by

the Examiner offers no apparent support for such a statement or conclusion. Specifically, the cited Column 5/6 text merely discloses the formation of the source drain 63/64 in the substrate, and the doping/size of these regions. The statement about small sheet resistance and better performance relates to the self alignment of the select gate to the floating gate and control gate, not to any alignment of the impurity regions (see Col. 6, lines 14-19). The cited Column 10 text states the small sheet resistance, small loading effect and faster performance result from the particular way the select gate is formed, and again not by any stated alignment to the impurity regions (see Col. 10, lines 57-67). Therefore, it is respectfully submitted that Chen '104 does not provide the requisite motivation for combining the teachings thereof with the device of Wang as suggested by the Examiner.

Since the combination of references relied upon by the Examiner fails to teach or suggest the claimed invention, and fails to provide a motivation for combining their teachings (in the case of Chen '104), the Applicant respectfully submits that claim 23 is not rendered obvious by Wang, Koh, and Chen '104.

3. Dependent Claim 24

Claim 24 depends upon claim 23, and is therefore considered allowable for the reasons set forth above.

C. Rejection of Claims 25 and 26 Under § 103(a)

Claims 25-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of admitted Prior Art Figure 1C.

Claims 25-26 depend from claim 23, and are therefore considered allowable for the reasons set forth above in Part B. The addition of Prior Art Figure 1C does not cure the deficiencies of Wang, Koh, and Chen '104.

D. Rejection of Claim 27 Under § 103(a)

Claim 27 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 5,751,048 (Lee).

Claim 27 depends from claim 23, and is therefore considered allowable for the reasons set forth in Part B above. The addition of Lee does not cure the deficiencies of Wang, Koh, and Chen '104.

E. Rejection of Claims 28 and 29 Under § 103(a)

Claims 28-29 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 6,140,182 (Chen '182).

Claim 28 recites an array of the memory cells that are recited in claim 23, including the first, second and third portions of the second insulation layer, the position of the control gate first portion relative to the second insulation layers first and second portions, and the alignment of the second region edge with the control gate vertical sidewall portion. The addition of Chen '182 does not appear to overcome the shortcomings of Wang, Koh, and Chen '104. Therefore, for the reasons set forth in Part B above, it is submitted that claim 28, along with claim 29 dependent thereon, are not rendered obvious by these references.

F. Rejection of Claims 30 and 31 Under § 103(a)

Claims 31-32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of admitted Prior Art Figure 1C. Claims 30-31 depend from claim 28, and are therefore considered allowable for the reasons set forth in Parts B and E above. The addition of Prior Art Figure 1C does not cure the deficiencies of Wang, Koh, Chen '104 and Chen '182.

G. Rejection of Claim 32 Under § 103(a)

Claim 32 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of Lee. Claim 32 depends from claim 28, and is therefore considered allowable for the reasons set forth in Parts B and E above. The addition of Lee does not cure the deficiencies of Wang, Koh, Chen '104 and Chen '182.

Conclusion

For all of these reasons, the Applicant respectfully submits that the rejections based upon 35 U.S.C. 103 are in error, and request the Board to affirm the patentability of the claims on appeal.

Respectfully submitted,

GRAY CARY WARE & FREIDENRICH

Dated: April 28, 2003 By: _____

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Reg. No. 39,749

Attorneys for Applicant(s)

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APPENDIX

23. (Twice Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region;

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

an electrically conductive control gate having a first portion disposed over the second insulation layer first portion and adjacent to the second insulation layer second portion, and a second portion extending over the second insulation layer third portion, the control gate having a substantially vertical sidewall portion; and

an insulation spacer formed adjacent to the substantially vertical sidewall portion of the control gate;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

24. The device of claim 23, further comprising:

a third insulation layer formed over a top surface of the control gate.

25. The device of claim 23, wherein the floating gate includes a sharp edge portion that extends toward the control gate.

26. The device of claim 25, the first and second portions of the control gate form a notch into which the sharp edge portion of the floating gate extends.

27. The device of claim 23, further comprising:

a layer of metalized silicon formed on the second region and aligned to the insulation spacer.

28. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region, and

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion and a second portion, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the control gate first portion is positioned over the second insulation layer first portion and adjacent to the second insulation layer second portion and the control gate second portion extends over the second insulation layer third portion, and wherein each of the control gates has a substantially vertical sidewall portion; and

a plurality of insulation spacers each formed adjacent to one of the substantially vertical sidewall portions of the control gates;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

29. The device of claim 28, further comprising:

a third insulation layer formed over a top surface of each of the control gates.

30. The device of claim 28, wherein each of the floating gates includes a sharp edge portion that extends toward one of the control gates.

31. The device of claim 30, wherein for each of the control gates, the first and second portions form a notch into which the sharp edge portion of the floating gate extends.

32. The device of claim 28, further comprising:

a layer of metalized silicon formed on each of the second regions and aligned to the corresponding insulation spacer.